CLAIMS

1. A focal plane array containing rows and columns of pixels for IR imaging, wherein pixel readout and analog to digital conversion is performed in an integrated circuit inclusive of said array, comprising:
   - at least one capacitor per pixel, accumulating the charge of a detector element.
   - at least one peripheral block comprising a comparator for on/off switching a digital controller, wherein said controller controls a digital to analog charge converter for providing an appropriate amount of charge to cancel out the charge of one pixel at a time by said at least one peripheral block.
   - switching elements for connecting said pixel capacitors to appropriate said peripheral blocks

2. A focal plane array for IR imaging as in claim 1 comprising a cycle generator, for controlling a charge output of a digital to analog converter to cancel out said charge of said pixel.

3. A focal plane array for IR imaging as in claim 2 wherein said cycle generator is a ramp generator connected through a capacitor to the input port of at least one of said peripheral blocks and to a column line.

4. A focal plane array for IR imaging as in claim 3 wherein said ramp generator produces at least one linear ramp.

5. A focal plane array for IR imaging as in claim 1 wherein said comparator includes an integrator as an input stage.

6. A focal plane array for IR imaging as in claim 1 and wherein said focal plane array is cooled.

7. A focal plane array for IR imaging as in claim 1 wherein a plurality of said peripheral blocks are grouped in groups, and wherein all said peripheral blocks belonging to one group operate simultaneously.

8. A focal plane array for IR imaging as in claim 7 and wherein each of said groups contains at least two of said peripheral blocks per each column.

9. A focal plane array for IR imaging as in claim 7 and wherein one multi ramp generator serves at least one group of said peripheral blocks.

10. A focal plane array for IR imaging as in claim 7 and wherein one counter serves at least one group of said peripheral blocks.

11. An IR imaging system as in claim 1 and wherein an external programmable logic device connected via a communication channel participates at least in the control of said peripheral blocks.

12. An IR imaging system as in claim 11 wherein said external programmable device also contains a buffer, for providing an interface between the readout stream and the timing parameters and communications protocols of a user.

13. A method for digitally quantifying IR radiation impinging on a focal plane array, wherein the charge accumulated in each pixel is simultaneously readout and analog to digital converted, employing at least one said peripheral block for each column of said array, and wherein a digital to analog charge converter is controlled by a comparator to supply a charge in an appropriate quantity to cancel out said charge of said pixel.

14. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 and wherein a cycle generated contains at least one ramp.

15. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 wherein an analog to digital conversion of the charge in every pixel is done on the focal plane in two quantification steps, a first step providing the most significant bits and a second step the least significant bits of said quantification

16. A method as in claim 15 wherein a dual ramp generator generates a dual step charge cancellation of said pixel charge, providing a most significant count in a first step and a least significant count in a second step.

17. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 15 and wherein the combination of the most significant bits and the least significant bits into one digital number is done partially externally, outside of said focal plane array.

18. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 16, and wherein a tradeoff between the resolution of said quantification and the frame rate is enabled by programming said dual ramp conversion cycle.

19. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13, and wherein the pixels of said array are grouped in rows, such that quantification is performed simultaneously for all members of said group, each group at a time, allocating at one conversion time one said peripheral block to each member of a group.

20. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 19, and wherein for said each group of pixels, one common ramp generator produces at least one linear voltage ramp whereby in each said peripheral block a low level DC

current is created by said ramp driving a capacitor connected to the junction of the pixel capacitor and input of said peripheral block.

21. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 19, and wherein each of said groups contain two rows of said array.